NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 600-60538-01.TGZ
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IS410 OR EQU1VALENT MUST CONFORM TO UL94V-0 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.
   D. ENSURE ALL THE VIA HOLES ARE FILLED WITH SOLDER MASK TO ENSURE GOOD QUALITY OF SILK SCREEN PRINT.

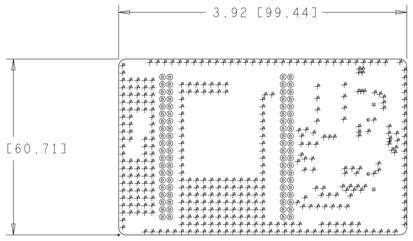
5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

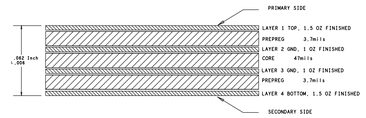
7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
⌀	12.0	+3.0/-3.0	PLATED	393
◎	39.37	+3.0/-3.0	PLATED	80
⊞	66.11	+3.0/-3.0	PLATED	2
⊕	46.063	+2.0/-2.0	NON-PLATED	2



SECTION A-A
SCALE: NONE
(X-SECTION VIEW / 4LAYER BOARD)

SINGLE ENDED

LAYER NO.	CONDUCTOR WIDTH	REFERENCE LAYER	IMPEDANCE +/-10%
LAYER 1	5.65 Mils	2	50-ohm +/-10%
LAYER 4	5.65 Mils	3	50-ohm +/-10%

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

MATERIAL 2
FINISH 7

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN HUSA	19/02/19
ENGINEER ANNR	19/02/19
CHECKER PRVE	19/02/19
QA -	-
PROJ. ENG. -	-

CYPRESS EMBEDDED IN TOMORROW
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE
PCB FABRICATION,
CYUSB3ACC-004A On-Semi Image Sensor ICB

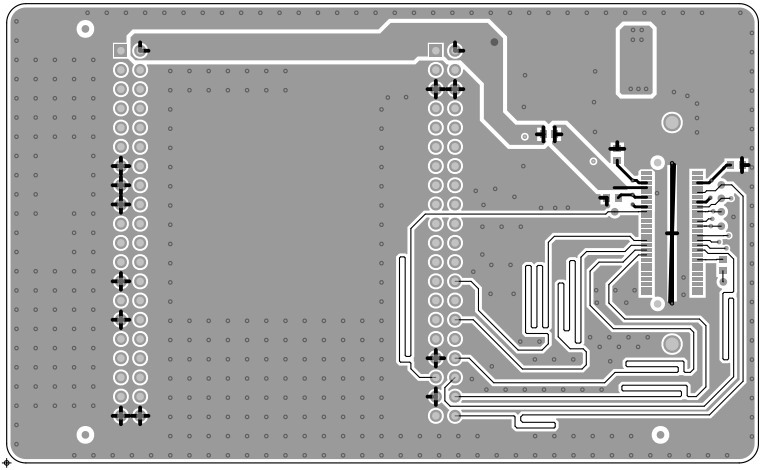
SIZE	CAGE CODE	CY P/N
D	-	610-60548-01

SCALE	SHEET	REV
1/1	1 OF 1	01

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

ALLEGRO FILE: 600-XXXXX-01_02.BRD

FAB NOTES REV 06/09/18



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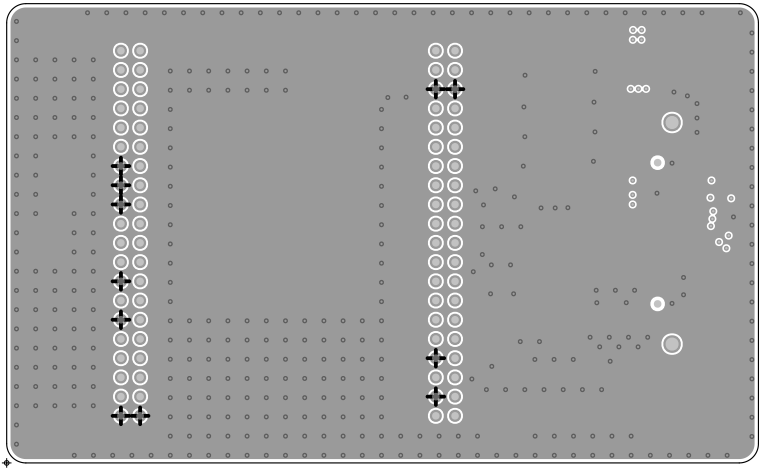
	DRAWN BY: HUSA		
	LAYER: PRIMARY SIDE		
	DWG NO: 600-60548-01	REV: 01	DATE: 19/02/19



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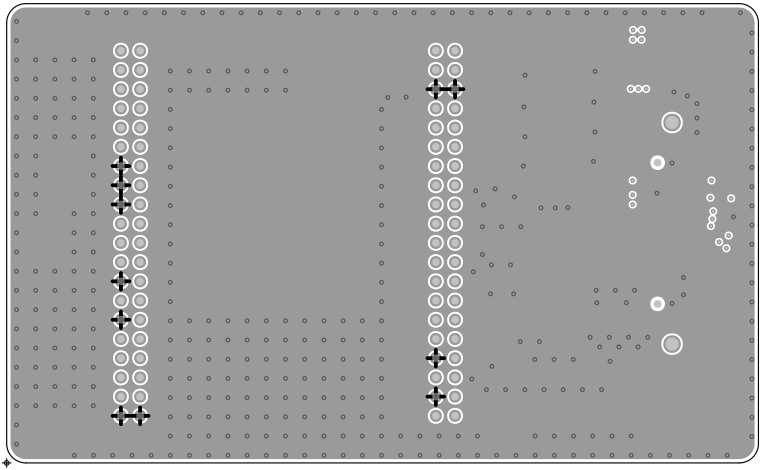
	LAYER: 02_GND1		
	DWG NO: 600-60548-01	REV: 01	DATE: 19/02/19



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	LAYER: 03_GND2		
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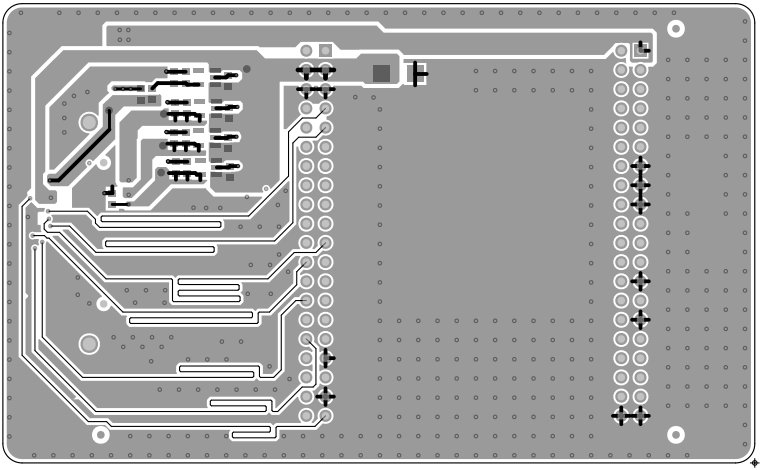

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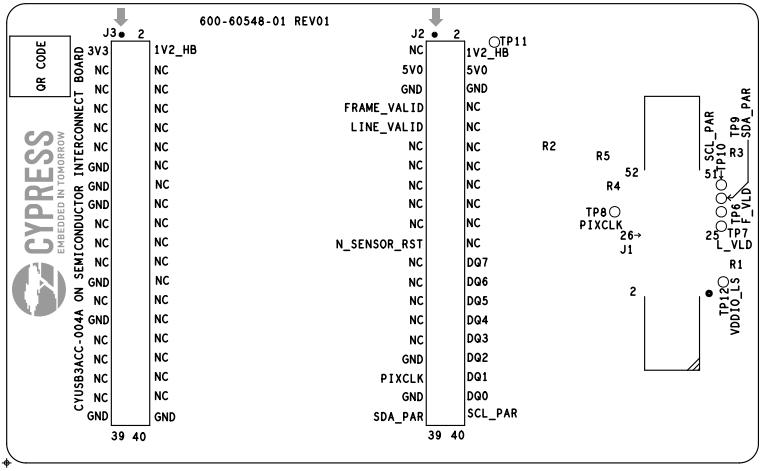
	LAYER: SECONDARY SIDE		
	DWG NO: 600-60548-01	REV: 01	DATE: 19/02/19



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: BOARD NAME: CYUSB3ACC-004A On-Semi Image Sensor ICB		
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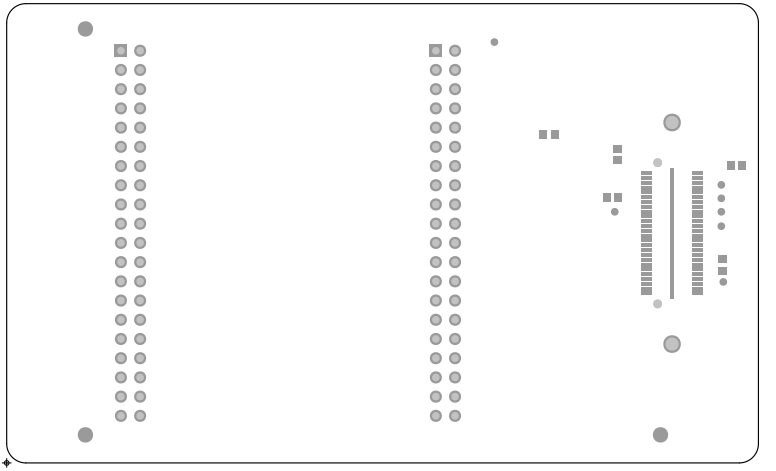

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	LAYER: PRIMARY SIDE SOLDERMASK		
	DWG NO: 600-60548-01	REV: 01	DATE: 19/02/19



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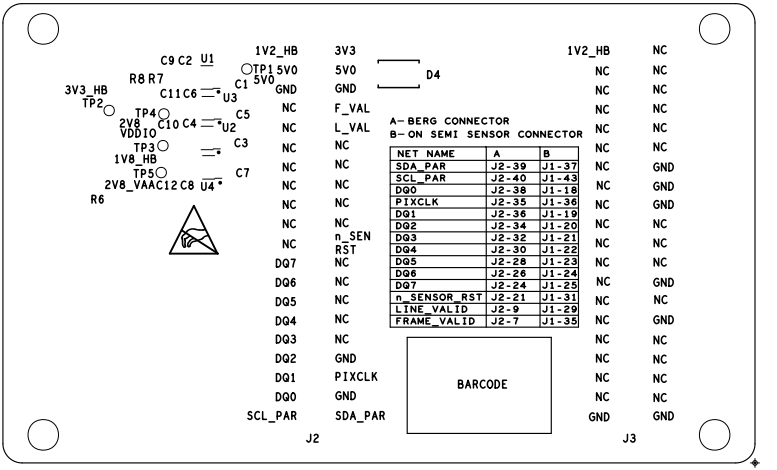

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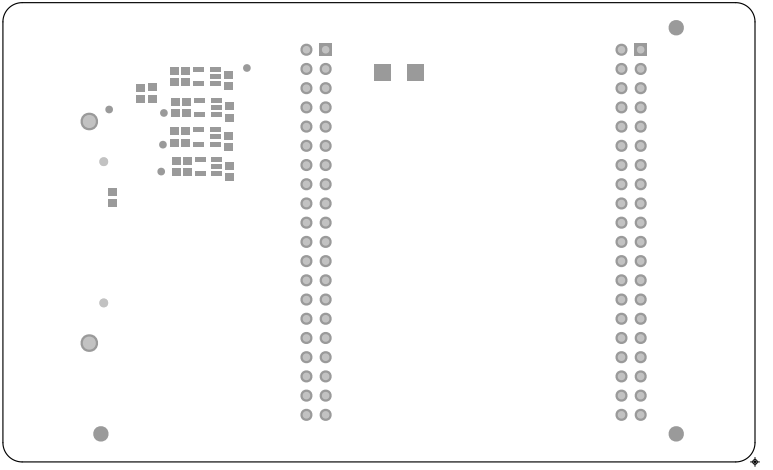

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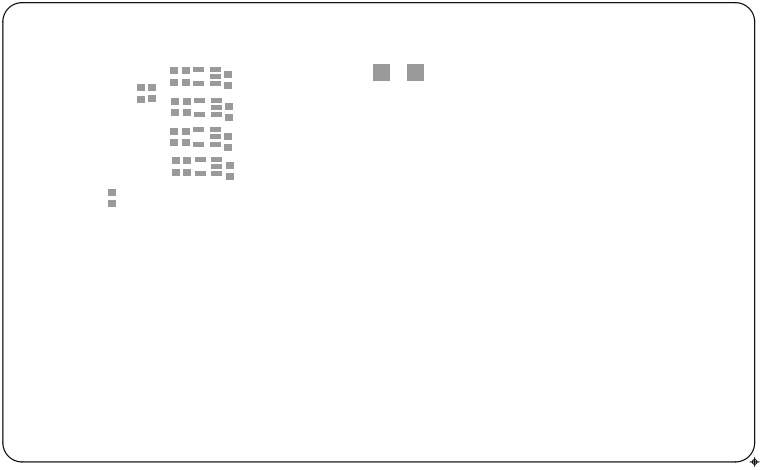

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